Amendments to the Specification

Please change the title of the invention as follows:

MULTI-LEVEL PATTERN HISTORY BRANCH PREDICTOR USING BRANCH PREDICTION ACCURACY HISTORY TO MEDIATE THE PREDICTED OUTCOME

Please remove the underline from the heading at page 1, line 6 as follows:

~~Field of the Invention~~   Field of the Invention

Please remove the underline from the heading at page 1, line 12 as follows:

~~Background of the Invention~~ Background of the Invention

Please replace the paragraph at page 2 lines 25 through 28 with the following rewritten paragraph:

Fig. 1 is a schematic diagram for illustrating a structure of a conventional two-level branch predictor. For example, the branch predictor is illustrated in Fig. 2 of *New Algorithm Improves Branch Prediction* by Linley Gwennap, March 27, 1995, ~~MOCROPROCESSOR~~ MICROPROCESSOR REPORT, pp. 17-21.

Please replace the paragraph at page 3 lines 6 through 13 with the following rewritten paragraph:

The pattern history table **20** is used for recording [[a]] pattern history bit$\underline{s}$ Sc, which ~~is~~ are used for predicting a conditional branch of a branch instruction to be performed in response to each pattern. For example, the two-level branch predictor predicts a conditional branch **I(Sc)** in response to an entry of 10 stored in the pattern history table **20**. The entry corresponds with a

pattern 111010 stored in the branch history register **10**. According to the predicted conditional branch **I(Sc)**, the next instruction to the branch instruction is fetched. Referring to the Gwennap paper referenced above, a predicted conditional branch **I(Sc)** is determined by a most significant bit (MSB) of [[a]] pattern history bit<u>s</u> **Sc** stored in the pattern history table **20**.

Please replace the paragraph at page 3 line 18 through page 4 line 3 with the following rewritten paragraph:

According to the real conditional branch **Rc**, both data of the branch history register **10** and the pattern history bit<u>s</u> **Sc** stored in the pattern history table **20** are changed. This process is described as follows. When a least significant bit (LSB) corresponding to the real conditional branch **Rc** of the branch instruction is stored to the branch history register **10**, the remaining bits are shifted to the left. At this time, the pattern history bit<u>s</u> **Sc** stored in the pattern history table **20** is updated in response to the real conditional branch **Rc**. For example, if the real conditional branch **Rc** is 1 denoting predict taken , the pattern history bit<u>s</u> **Sc** [[is]] <u>are</u> increased by 1 , and if the real conditional branch **Rc** is 0 denoting predict not taken , the pattern history bit<u>s</u> **Sc** [[is]] <u>are</u> decreased by 1 . The pattern history bit<u>s</u> **Sc** can be composed of an up/down saturating counter as shown in *A Study of Branch Prediction Strategies* , by J. Smith, May 1981, pp. 135-148. The saturating counter maintains a minimal value of [[a]] pattern history bit<u>s</u> **Sc** when the pattern history bit<u>s</u> **Sc** [[is]] <u>are</u> the minimal value, although the real conditional branch **Rc** is 0 denoting not taken . In addition, the saturating counter maintains a maximum value of [[a]] pattern history bit<u>s</u> **Sc** when the pattern history bit<u>s</u> **Sc** [[is]] <u>are</u> the maximum value, although the real conditional branch **Rc** is 1 denoting taken .

Please remove the underline from the heading at page 4, line 22 as follows:

~~Summary of the Invention~~	<u>Summary of the Invention</u>

Please remove the underline from the heading at page 5, line 7 as follows:

~~Brief Description of the Drawings~~ | A8 Brief Description of the Drawings

Please remove the underline from the heading at page 5, line 18 as follows:

~~Description of the Preferred Embodiment~~ | Description of the Preferred Embodiment A9

Please replace the paragraph at page 5 lines 19 through 26 with the following rewritten paragraph:

A10

In accordance with the invention, a branch predictor outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on [[an]] <u>one or more</u> accuracy history bit<u>s</u>. According to the accuracy history bit<u>s</u>, it is determined whether the branch prediction outcome of the branch predictor is correct. If the predicted conditional branch is correct, the branch predictor outputs the predicted conditional branch, and if the predicted conditional branch is not correct, the branch predictor outputs the inverted predicted conditional branch, in response to the predicted accuracy history signal.

Please replace the paragraph at page 5 line 27 through page 6 line 4 with the following rewritten paragraph:

A11

Fig. 2 is a schematic diagram illustrating a structure of one embodiment of a two-level branch predictor according to the present invention. Referring to **Fig. 2**, the two-level branch predictor comprises a branch history register **15** for recording actions of the most recent k conditional branches, a pattern history table **25** for recording [[a]] pattern history bit<u>s</u> **Sc** used for generating a predicted conditional branch **I(Sc)**, and an accuracy history table **60** for recording accuracy history of the predicted conditional branch **I(Sc)**. The accuracy history table **60** is

A\11   composed of a memory array.

Please replace the paragraph at page 6 lines 5 through 9 with the following rewritten paragraph:

A\12   A first state transition logic circuit **30** generating [[a]] pattern history bits **Sc** to be stored to the pattern history table **25** in response to a real conditional branch **Rc** is coupled to the pattern history table **25**. In addition, a second state transition logic circuit **50** generating [[an]] accuracy history bits **Ac** to be stored to the accuracy history table **60** is coupled to the accuracy history table **60**.

Please replace the paragraph at page 6 lines 10 through 18 with the following rewritten paragraph:

A\13   Further, the branch predictor according to the present invention comprises a comparator **40** generating a comparison signal by comparing the predicted conditional branch **I(Sc)** generated by the pattern history bits **Sc** with the real conditional branch **Rc** of the branch instruction. The comparison signal is inputted to the second state transition logic circuit **50** to generate the accuracy history bits **Ac**. In addition, the branch predictor comprises a multiplexer **70** selecting either a predicted conditional branch **I(Sc)** or an inverted predicted conditional branch as a final branch prediction outcome or result. A predicted accuracy history signal **I(Ac)** based on the accuracy history bits **Ac** is used as a selection signal for the multiplexer **70**. Operation of the branch predictor is described as follows.

Please replace the paragraph at page 6 lines 19 through 21 with the following rewritten paragraph:

A14

A predicted conditional branch **I(Sc)** is generated in response to [[a]] pattern history bit**s** Sc corresponding to a pattern stored in the branch history register **15**. The predicted conditional branch **I(Sc)** is inputted to the comparator **40** to be compared with a real conditional branch **Rc**.

Please replace the paragraph at page 6 line 22 through page 7 line 1 with the following rewritten paragraph:

The real conditional branch **Rc** has a 1 or 0 value according to "predict taken" or "predict not taken," respectively, and the value stored in the branch history register **15** is updated in response to the value of the real conditional branch **Rc**. According to the updated value of the branch history register **15**, the pattern history bit**s** Sc [[is]] **are** updated. The first state transition logic circuit **30** updates the pattern history bit**s** Sc. The first state transition logic circuit **30** is composed of an up/down saturating counter. In the first state transition logic circuit **30**, the value of the pattern history bit**s** Sc [[is]] **are** increased by 1 when the real conditional branch **Rc** is 1 (i.e., taken), and the value of the pattern history bit**s** Sc is decreased by 1 when the real conditional branch **Rc** is 0 (i.e., not taken).

Please replace the paragraph at page 7 lines 2 through 8 with the following rewritten paragraph:

A15

The predicted conditional branch **I(Sc)** has a value of 1 or 0 in response to a most significant bit (MSB) of the pattern history bit**s** Sc. The comparator **40** outputs 1 or 0 as a comparison signal to the second state transition logic circuit **50** by comparing the real conditional branch **Rc** and the predicted conditional branch **I(Sc)**. For example, if the predicted conditional branch **I(Sc)** is the same as the real conditional branch **Rc**, the comparator **40** outputs 1, and if

A15

the predicted conditional branch **I(Sc)** is different from the real conditional branch **Rc**, the comparator **40** outputs 0 .

Please replace the paragraph at page 7 lines 9 through 16 with the following rewritten paragraph:

A16

The second state transition logic circuit **50** receiving the comparison signal determines [[an]] accuracy history bit_s **Ac** to be stored to the accuracy history table **60** in response to the comparison signal. The second state transition logic circuit **50** is composed of an up/down saturating counter increasing the value of the accuracy history bit_s **Ac** by 1 when the predicted conditional branch **I(Sc)** is the same as the real conditional branch **Rc**, and decreasing the value of the accuracy history bit_s **Ac** by 1 when the predicted conditional branch **I(Sc)** is different from the real conditional branch **Rc**. The accuracy history bit_s **Ac** can be used after learning a branch accuracy of the corresponding pattern by monitoring the pattern.

Please replace the paragraph at page 7 line 17 through page 8 line 3 with the following rewritten paragraph:

A17

According to the above described method, the accuracy history bit_s **Ac** [[is]] are determined and stored to the accuracy history table **60**. According to the accuracy history bit_s **Ac**, it can be determined whether a prediction result of the branch predictor is correct. For example, if [[a]] pattern history bit_s **Sc** [[is]] are 011 corresponding to a pattern 11 10 stored in the branch history register **15**, a predicted accuracy history signal **I(Ac)** is generated by an MSB of the accuracy history bit_s **Ac**. The predicted accuracy history signal **I(Ac)** is used for determining whether the predicted conditional branch **I(Sc)** is correct. For example, if it is considered as the predicted conditional branch **I(Sc)** is correct, the predicted accuracy history signal **I(Ac)** having a value of 1 is outputted to the multiplexer **70**. Thus, the predicted conditional branch **I(Sc)** is

outputted from the multiplexer **70** as a final prediction result. In addition, if it is considered as the predicted conditional branch **I(Sc)** is not correct, the predicted accuracy history signal **I(Ac)** having a value of 0 is outputted to the multiplexer **70**. Thus, the inverted predicted conditional branch is outputted from the multiplexer **70** as a final prediction result. As described above, the predicted accuracy history signal **I(Ac)** is used as a selection signal of the multiplexer **70** selecting either the predicted conditional branch **I(Sc)** or an inverted predicted conditional branch as a final prediction outcome of the branch predictor.

Please replace the paragraph at page 8 lines 4 through 12 with the following rewritten paragraph:

As described above, the branch predictor according to the present invention outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on [[an]] accuracy history bits, so that the two-level branch predictor can reduce the misprediction and a microprocessor can process branch instructions more efficiently. In this case, the branch prediction according to the present invention merely appends the accuracy history table **60** and multiplexer **70** to the conventional branch predictor. Thus, the branch prediction according to the present invention can reduce the misprediction with relatively simple circuitry and low hardware cost.

Please remove the underline from the heading at page 11, line 1 as follows:

~~Abstract of the Disclosure~~ | Abstract of the Disclosure

Please replace the paragraph at page 11 lines 4 through 14 with the following rewritten paragraph:

A20

A branch predictor outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on [[an]] <u>one or more</u> accuracy history bit<u>s</u>. According to the accuracy history bit, it is determined whether the branch prediction outcome of the branch predictor is correct. If the predicted conditional branch is correct, the branch predictor outputs the predicted conditional branch, and if the predicted conditional branch is not correct, the branch predictor outputs the inverted predicted conditional branch, in response to the predicted accuracy history signal. For performing this process, the branch prediction appends an accuracy history table and a multiplexer to a conventional branch predictor, so that the branch prediction according to the present invention can reduce the misprediction with relatively simple circuitry and low hardware cost.

Please remove the underline from the heading at page 9, line 1 as follows:

~~CLAIMS~~ A21   CLAIMS